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☐	L23	L21 same (phase near3 shift$4)	1
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L32: Entry 3 of 5 File: USPT Nov 2, 1999

DOCUMENT-IDENTIFIER: US 5978926 A

**** See image for Certificate of Correction ****

TITLE: Processor chip for using an external clock to generate an internal clock and for using data transmit patterns in combination with the internal clock to control transmission of data words to an external memory

Detailed Description Text (6):

External clock generator 35 includes a PLL 60, a clock divider 62, an initial synchronization circuit 65, a multiplexer 67, a 90.degree. phase shifter 68, and a final synchronization circuit 70. The PLL receives MasterClock at a first input and generates an internal signal at 4x. The clock divider divides this signal by factors of 4, 6, and 8, and provides signals at 1x, 2/3x, and 1/2x. These signals are synchronized and one of the three is selected at the multiplexer on the basis of a desired external clock divisor (programmable at boot time). The selected signal, and a version thereof that is phase shifted by a quarter cycle are again synchronized to generate an internal signal SClock, an external signal TClock in phase with SClock, and an external signal RClock that leads TClock by a quarter cycle, all three at the same selected frequency (1x, 2/3x, or 1/2x). An additional signal 1x(ND) is used to generate two external signals SyncOut and MasterOut, both at 1x, regardless of the selected frequency. SyncOut (at 1x) is fed back via an external circuit board trace to a SyncIn input pin on the chip and then to a second input of PLL 60 for overall synchronization.

Current US Cross Reference Classification (1):

713/500

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L30: Entry 1 of 1 File: USPT Apr 8, 2003

DOCUMENT-IDENTIFIER: US 6546516 B1
TITLE: Method and apparatus for measuring timing characteristics of message-oriented transports

Brief Summary Text (12):
According to the invention, there is provided a means of accurately measuring timing characteristics of bursty message traffic over relatively low to moderate rate digital transports such as the Musical Instrument Digital Interface (MIDI). The apparatus includes means for generating a reference pulse stream, such as a sequencer. A transcoder device receives the reference pulse stream and routs the pulse stream to a device under test and, in analog form, to a first channel input of a digital recording device, such as a sound card installed in a personal computer. The transcoder also receives an output pulse stream from the device under test and routes the output pulse stream, in analog form, to a second channel input of the digital recording device. The invention provides the following advantages: Low hardware cost, Highly accurate timing measurements, Differential technique that allows timing errors in the reference pulse stream to be eliminated from measurements, and Easily supports a broad variety of analysis techniques using common software on personal computers.

Current US Cross Reference Classification (1):
710/60

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L32: Entry 1 of 5 File: USPT Jan 6, 2004

DOCUMENT-IDENTIFIER: US 6675249 B2
TITLE: Information processing equipment and information processing system

Detailed Description Text (20):
M-phase clock CLKi [where i is 0 to M-1] with each clock pulse in phase shifted by 1/M cycle is obtained by modifying the synchronous signal generating circuit 25 or being input externally. CLK0 is assumed the internally operating clock CLK. The external bus access timing signal generating circuit 24 is modified; M lines instead of two signals SET0 and SET1 shown in FIG. 5 are required and they are represented as SETi.

Current US Original Classification (1):
710/305

Current US Cross Reference Classification (1):
713/400

CLAIMS:

7. The information processing equipment according to claim 6, wherein: the bus I/O signal conversion circuit comprises: a circuit for generating a select signal whose state changes per one or more cycles from the timing signals generated by the external bus access timing signal generating circuit, M-1 pieces of latches for holding a signal input from the external bus, while being clocked by M-phase clock pulses with each in phase shifted by 1/M cycle, a latch for holding a signal to enter the internal selected in accordance with the select signal from among the signal input from the external bus and the signals output from the M-1 pieces of latches, while being clocked by the internal clock.

13. The information processing equipment according to claim 12, wherein: the bus I/O signal conversion circuit comprises: a circuit for generating a select signal whose state changes per one or more cycles from the timing signals generated by the external bus access timing signal generating circuit; M-1 pieces of latches for hold a signal input from the external bus, while being clocked by M-phase clock pulses with each in phase shifted by 1/M cycle, a latch for holding a signal to enter the internal selected in accordance with the select signal from among the signal input from the external bus and the signals output from the M-1 pieces of latches, while being clocked by the internal clock.

L32: Entry 2 of 5 File: USPT Jan 29, 2002

DOCUMENT-IDENTIFIER: US 6343364 B1
TITLE: Method and device for local clock generation using universal serial bus downstream received signals DP and DM

Brief Summary Text (18):
A method having features of the present invention comprises a method for generating a local clock signal in a device using Universal Serial Bus downstream signals DP and DM, comprising receiving the USB downstream differential signals DP and DM and generating a downstream bit-serial signal from the USB downstream signals, counting a number of cycles R of a free-running high frequency clock signal contained within a known number of bit periods S of the received downstream bit-serial signal, dividing the counted number of cycles R of the free-running high frequency clock signal by the known number of bit periods S of the received downstream bit-serial signal for determining a resultant number of the free-running high frequency clock cycles T contained within a single bit period of the received downstream bit-serial signal, and generating a local clock signal having a period equal to the number of free-running high frequency clock cycles T. The step of generating the local clock signal may comprise counting the number of the free-running high frequency clock cycles T to generate a period of the local clock signal, and initializing the counting step when there is a data toggling in the received downstream bit serial signal for locking in phase the generated local clock with the received downstream bit serial signal. The step of generating the local clock signal may further comprise updating the period of the local clock signal when a known received downstream bit serial pattern is recognized. The known number of bit periods S of the received downstream bit-serial signal may be eight. The method may further comprise generating the free-running high frequency clock signal with a ring oscillator. The step of generating the free-running high frequency clock signal with a ring oscillator further may comprise generating an even number of signals V having a period of the free-running high frequency clock signal and the phase shifted of 360.degree./V. The even number of signals V may be eight. The method may be implemented in an integrated circuit module. The integrated circuit module may be positioned on a smart card. The local clock signal may be phase locked with the downstream bit serial signal at least once every seven bit periods of the downstream bit serial signal by the use of bit-stuffing. The counting step may be performed during a period of time when the downstream bit serial signal comprises a Sync byte and a PID Setup byte of a USB Token Packet and Data Packet. The known received downstream bit serial pattern may comprise a Sync byte and a PID Setup byte of a USB Token Packet and Data Packet. The method may further comprise a step for determining if T is within predefined limits. The local clock signal may be used to sample the USB received downstream serial bit data and to time the USB transmitted upstream serial bit data.

Brief Summary Text (19):
In an alternate embodiment of the invention, a device containing a circuit for generating a local clock signal using Universal Serial Bus downstream signals DP and DM, comprises means for receiving the USB downstream differential signals DP and DM and generating a downstream bit-serial signal from the USB downstream signals, means for counting a number of cycles R of a free-running high frequency clock signal contained within a known number of bit periods S of the received downstream bit-serial signal, means for dividing the counted number of cycles R of

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L8: Entry 3 of 10 File: USPT Mar 30, 1999

DOCUMENT-IDENTIFIER: US 5889728 A
TITLE: Write control method for memory devices

Detailed Description Text (26):
The present invention provides advantages over schemes of the past by using the combine control signals (CCS) block 90. Notably, the CCS block 90 has comparable complexity with the control blocks used in prior 8-bit internal word-format memories, and yet is still able to accommodate the multitude of possibilities to initiate and/or end a write using the multiple write control signals, instead of just a write enable and/or chip enable signal. Further, the present invention provides stable, balanced (aligned over the multiple write control signals) and improved write parameter margins over a large range of technology, temperature and/or supply voltage corners, especially when driving a circuit which ATD-gates the data write bus to bitline access. This is a major advantage over conventional schemes which provide control logic targeted to drive data write bus to bitline interfaces gated only by a combination of addresses or which use unstabilized trip point input buffers. In addition, the present invention provides improved write parameter margins in spite of resorting to a simple data write driver whereas schemes of the past relied on relatively complex data-latched drivers, combined data write driver/level restoring circuits, address-only gated data write bus to bitline interfaces or internal write pulse edge timing and slope adjustment.

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L8: Entry 4 of 10 File: USPT May 26, 1998

DOCUMENT-IDENTIFIER: US 5757381 A
TITLE: Methods for fast scrolling of images

Detailed Description Text (31):
SCSI controller 122 is connected to a SCSI processing circuit 124. SCSI processing circuit 124 is connected to bus interface 106 and a timing adjustment circuit 130. SCSI processing circuit 124 performs the following operations: (1) receives commands and status information from CPU 604 via bus interface 106; (2) controls hard disk 638 (through SCSI controller 122) in accordance with these commands and status information; (3) in cooperation with timing adjustment circuit 130, transfers data to and from a RAM processing circuit 132; and (4) sends status information to CPU 604 via bus interface 106. For example, SCSI processing circuit 124 can activate and deactivate the transfer of data to and from hard disk 638. The status signals generated by SCSI processing circuit 124 could be used by data transfer driver 714 which is designed to work with data transfer device 110.

Detailed Description Text (36):
RAM processing circuit 132 comprises a switch 134 for connecting RAM A and RAM B on one hand to timing adjustment circuit 130 and bus interface 106 on the other hand. Specifically, if it is desirable to transfer data between SCSI processing circuit 124 to either RAM A or RAM B, switch 134 causes timing adjustment circuit 130 to be connected to the appropriate memory. Similarly, if it is desirable to transfer data between internal RAM to either RAM A or RAM B, switch 134 causes bus interface 106 to be connected to the appropriate memory device in data transfer device 110. It should be note that RAM A may be connected to either timing adjustment circuit 130 or bus interface 106 at a given time, but cannot be simultaneously connected to both timing adjustment circuit 130 and bus interface 106. Similarly, RAM B may be connected to either timing adjustment circuit 130 or bus interface 106 at a given time, but cannot be simultaneously connected to both timing adjustment circuit 130 and bus interface 106. Also, data cannot be directly transferred between timing adjustment circuit 130 and bus interface 106. The detailed operation of switch 134 in connection with the transfer of data will be described below.

Detailed Description Text (41):
In one embodiment of the present invention, SCSI processing circuit 124, RAM processing circuit 132, timing adjustment circuit 130, and bus interface 106 are fabricated on a single semiconductor chip 140.

L8: Entry 1 of 10 File: USPT Sep 28, 2004

DOCUMENT-IDENTIFIER: US 6799304 B2
TITLE: Arbitration within a multiport AMBA slave

Detailed Description Text (13):
The circuit 138 may be implemented as a state machine circuit or block. In one embodiment, the state machine circuit 138 may be implemented as a port grant state machine circuit. The port grant state machine circuit 138 may be configured to control a handshake mechanism between the TDM arbiter circuit 104 and the individual AHB bus interface circuits 102a-n to adjust a timing in granting access to the peripheral controller circuit 108. The port grant state machine circuit 138 may be coupled to the arbitration kernel logic circuit 136 to receive information regarding which port (AHB bus interface circuit) 102a-n may be receive the grant.

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L10: Entry 2 of 15 File: USPT Aug 17, 1999

DOCUMENT-IDENTIFIER: US 5940114 A

** See image for Certificate of Correction **

TITLE: Image forming apparatus for correcting positional deviations of an image

Detailed Description Text (33):

Next, the maximum value MAX and the minimum value MIN of the N registration deviation data for each color are computed (S210). The difference between the maximum value MAX and the registration deviation data Di is calculated to eliminate image pattern read errors, and a check is made whether the difference is larger than a predetermined value k in all N-1 registration deviation data (S211). If it is determined that the difference is larger than the predetermined value k in all N-1 registration deviation data, the maximum value MAX is regarded to be an image pattern read error, ano this maximum value MAX is discarded from the registration deviation data (S212). If, however, the difference between the maximum value MAX and the registration deviation data Di is smaller than the predetermined value k in any of the N-1 registration deviation data, the maximum value MAX is left unchanged.

Detailed Description Text (34):

Next, the difference between the minimum value MIN and the other registration deviation data Di is calculated to eliminate image pattern read errors. A check is made to determine whether the difference is larger than the predetermined value k in all N-1 (N-2 when the maximum value MAX is discarded) registration deviation data (S213). If it is determined that the difference is larger than the predetermined value k in all N-2 or N-1 registration deviation data, the maximum value MAX is regarded to be an image pattern read error, and this maximum value MIN is discarded from the registration deviation data (S214). If, however, the difference between the maximum value MAX and the registration deviation data Di is smaller than the predetermined value k in any of the N-2 or N-1 registration deviation data, the maximum value MIN is left unchanged.

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L43: Entry 1 of 8 File: USPT Dec 10, 2002

DOCUMENT-IDENTIFIER: US 6493396 B1
** See image for Certificate of Correction **
TITLE: Phase shift key burst receiver having improved phase resolution and timing and data recovery

CLAIMS:

20. A communications system comprising: a transmitter for transmitting at a symbol rate phase shift key modulated burst signals including I and Q components on a transmission medium, the burst signals including a prefix portion and a data portion, I and Q components of the prefix portion being maintained at a predetermined relationship during at least a portion of the prefix portion; and a receiver for receiving the phase shift key modulated burst signals from the transmission medium, the receiver comprising an IF section for mixing received burst signals to an intermediate frequency signal, the intermediate frequency signal having a phase, an I-Q demodulator that includes a demodulator frequency generator for generating a demodulating signal having a frequency equal to or an integer multiple of the intermediate frequency signal to thereby extract the baseband I and Q components of the received burst signals, the demodulating signal having a phase, a phase adjustment circuit, responsive to the I and Q components that are maintained at the predetermined relationship, for adjusting the phase of the demodulating signal so that it is substantially in phase with the intermediate frequency signal, and a state-determining circuit for determining the respective states of baseband I and Q components of the phase shift key modulated signals, the state-determining circuit comprising a clock generator circuit for generating a symbol clock signal at the symbol rate, an analog-to-digital converter for sampling each of the baseband I and Q components at a predetermined rate to generate a first digital sample output stream from the baseband I component and a second digital sample output stream from the baseband Q component, each digital data sample of the first digital sample output stream being indicative of a logic state of the baseband I component at a respective sample time and each digital data sample of the second digital sample output stream being indicative of a logic state of the baseband Q component at a respective sample time, the predetermined rate being at least twice the Nyquist frequency of the baseband I and Q components, and a voter circuit receiving the first and second digital data sample streams, and, in response to occurrence of the symbol clock signal, comparing a current digital sample of the first digital data sample output stream to prior and subsequent digital data samples of the first digital data sample output stream to provide an I state signal output based on the majority logic state of the digital samples of the first digital data output stream that are compared and, in response to occurrence of the symbol clock signal, comparing a current digital data sample of the second digital data sample output stream to prior and subsequent digital data samples of the second digital data sample output stream to provide a Q state signal output based on the majority logic state of the digital samples of the second digital data output stream that are compared.

25. A receiver for receiving phase shift key modulated burst signals transmitted at a symbol rate including I and Q components, the burst signals including a prefix portion and a data portion, the I and Q components of the prefix portion being maintained at a predetermined relationship during at least a portion of the prefix

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L43: Entry 2 of 8 File: USPT Dec 26, 1995

DOCUMENT-IDENTIFIER: US 5479456 A
TITLE: Automatic false synchronization correction mechanism for biphase-modulated signal reception

Abstract Text (1):
An arrangement comprising a controllable clock signal source (1), a decision circuit (8) for determining the polarity of a received biphase signal at two successive sampling instants in a single symbol interval, and a phase detector (35) with a first comparator (16) to compare the polarity samples at the two sampling instants with each other. The phase detector generates a control signal for adjusting the frequency and phase of the adjustable clock signal source (1) in response to the output signal of the first comparator. A second comparator (28) compares polarity samples at the same relative sampling instant in two successive sampling instants with each other. The second comparator (28) inhibits phase detector (35) in response to the output signal of this second detector. In the case of false synchronization, the output of phase detector (35) will continue to present the same signal value, so that automatically an adjustment is made of the instant of correct synchronization. This adjustment is carried out by a VCO (3) and/or phase shifter means (12).

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L43: Entry 4 of 8 File: USPT Oct 27, 1992

DOCUMENT-IDENTIFIER: US 5159291 A
** See image for Certificate of Correction **
TITLE: Digitally controlled timing recovery loop with low intrinsic jitter and high jitter tolerance

Parent Case Text (14):
To overcome limitations in the prior art, and to overcome other limitations that will become apparent upon reading and understanding the present specification, the present invention discloses a timing recovery loop which tolerates a relatively large amount of incoming jitter and minimizes data dependent, ISI-induced, intrinsic jitter. The timing recovery loop is comprised of an oscillator with clock phase selection for generating a clock signal, wherein the oscillator accepts an adjust signal and a direction signal to control the degree and direction of phase shift in the clock signal, thereby causing it to speed-up and slow-down as required. Means are provided for sampling and comparing pulse amplitudes in the input signal so that a plurality of speed-up and slow-down signals can be generated in response thereto indicating an amount and direction of pulse position distortion in the input signal. A triple loop structure, controlled by a selection signal to operate in either a jitter tolerance mode or a bandwidth controlling mode, translates the speed-up and slow-down signals into the adjust and direction signals, and transmits the adjust and direction signals to the oscillator to eliminate jitter due to pulse position distortion in the input signal.

Detailed Description Text (58):
In summary, a timing recovery loop has been described which tolerates a relatively large amount of incoming jitter and minimizes data dependent, ISI-induced, intrinsic jitter. The timing recovery loop is comprised of an oscillator 16 with clock phase selection for generating a clock signal, wherein the oscillator accepts an adjust signal and a direction signal to control the degree and direction of phase shift in the clock signal, thereby causing it to speed-up and slow-down as required. A sampling phase comparator 10 and quarter bit detector 170 are provided for sampling and comparing pulse amplitudes in the input signal so that a plurality of speed-up and slow-down signals can be generated in response thereto indicating an amount and direction of pulse position distortion in the input signal. A triple loop structure, controlled by a selection signal to operate in either a jitter tolerance mode or a bandwidth controlling mode, translates the speed-up and slow-down signals into the adjust and direction signals, and transmits the adjust and direction signals to the oscillator 16 to eliminate jitter due to pulse position distortion in the input signal.